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AN EFFICIENT FAST DHT ALGORITHM FOR VLSI IMPLEMENTATION USING SPLIT RADIX ALGORITHM

M.TAMILSELVI[1] & A.LAKSHMINARAYANAN[2]

[1]PG Scholar, Department of Electronics and Communication Engineering, Kongunadu College of Engineering and Technology, Trichy, Tamil Nadu, India

[2]Assistant Professor, Department of Electronics and Communication Engineering, Kongunadu College of Engineering and Technology, Trichy, Tamil Nadu, India

ABSTRACT

A new very large scale integration (VLSI) algorithm for a 2N-length discrete Hartley transform (DHT) that can be efficiently implemented on a highly modular and parallel VLSI architecture having a regular structure is presented. The DHT algorithm can be efficiently split on several parallel parts that can be executed concurrently. Moreover, the proposed algorithm is well suited for the subexpression sharing technique that can be used to significantly reduce the hardware complexity of the highly parallel VLSI implementation.

KEYWORDS: Discrete Hartley Transform (DHT), DHT Domain Processing, Fast Algorithms